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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,812	03/22/2004	Raul Alejandro Perez	TI-36957	1062

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/805,812	PEREZ, RAUL ALEJANDRO	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-5, 10, 11, 16 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 is misdescriptive and rendered the claim in definite. it is seen that error amplifier recited in line 5 is separated from the main current loop. However, as shown in the drawing, the error amplifier is part of the main current loop.

Claims 3, 10 and 16 are indefinite because it is unclear as what impedance level is considered as low.

Claims 4, 11 and 17 are indefinite because it is unclear as what impedance level is considered as high.

Claims 2-5 are rejected as including the indefiniteness of claim 1.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Kadanka (USP 6556083).

As to claim 1, Kadanka discloses in figure 2 a method of stabilizing two current loops within a circuit comprising the steps of : providing a main current loop (loop comprising 12, 50, R1, R2, 40) for supplying current to a load (Rload); providing a sensing loop (loop comprising 22, 16, 14) for monitoring the current to the Iload; an error amplifier (12) coupled to the output of the sensing loop such that the capacitance of each loop is isolated from that of the other loop; and providing capacitance (40 and 14) to each loop whereby stability is independently maintained for each loop within selected operational criteria.

As to claim 2, figure 2 shows the step of coupling the output of the error amplifier to the gate of a transistor (18) and coupling the output of the sensing loop to the source of the transistor.

Insofar as understood to claim 3, figure 2 shows that the output of the main loop comprises a low impedance node.

Insofar as understood to claim 4, figure 2 shows that the output of the main loop comprises a high impedance node.

As to claim 5, figure 2 shows that the main loop comprises a low dropout regulator (LDO).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadanka (USP 6556083) in view of Chen (USP 6788143).

As to claim 6, Kadanka's figure 2 shows a circuit having a low capacitive load (40) and comprising two stable current loop sub circuits further comprising: a main current loop (loop comprising 12, 50, R1, R2, 40) for supplying current to the load; a sensing loop (loop comprising 22, 16, 14) for monitoring the current to the load, the sensing loop having a second compensation capacitor (14) for maintaining stability within a pre-selected operational range. Thus, figure 2 shows all limitations of the claim except for the detail of the differential amplifier 12. However, Chen's figure 1 shows a differential amplifier having the advantage of low power consumption. Therefore, it would have been obvious to one having ordinary skill in the art to use Chen's amplifier for Kadanka's amplifier for the purpose of improving the performance of the circuit. Thus, the modified kadanka's figure 2 further shows that the main current loop having a first compensation capacitor (Chen's C11) for maintaining stability within a pre-selected operational range; and a transistor (18) for coupling the output of the main current loop and the output of the sensing loop such that the first compensation capacitor is isolated from the second compensation capacitor.

As to claim 7, figure 2 shows that the transistor further comprises a MOSFET.

As to claim 8, the modified Kandaka's figure 2 fails to show that the transistor further comprises a bipolar transistor. However, it is well known in the art that bipolar transistor having equivalent function with FET. Therefore, it would have been obvious to one having ordinary

skill in the art use bipolar transistors for the modified Kandaka's figure 2 due to doctrine equivalent of function.

As to claim 9, the modified Kandaka's figure 2 shows that the output of the error amplifier is coupled to the gate of the transistor and the output of the sensing loop is coupled to the source of the transistor and to the second compensation capacitor.

As to claim 10, the modified's figure 2 shows that the main loop further comprises an error amplifier (12) and wherein the output of the main loop comprises a low impedance node of the error amplifier.

As to claim 11, the modified's figure 2 shows that the main loop further comprises an error amplifier (12) and wherein the output of the main loop comprises a high impedance node of the error amplifier.

As to claim 12, figure 2 shows that the main loop further comprises a low dropout regulator (LDO).

As to claim 13, the modified Kandaka's figure 2 fails to shows that the load capacitance of the circuit is on the order of approximately 1uF. However, it is well known in the art that the capacitance of the load capacitor determines the stability level of the output voltage. Furthermore, the particular capacitance level is seen as an obvious matter of preference bounded by well known manufacturing constraints and ascertainable by routine experimentation. The particular claimed relative current level limitations do not distinguish over the prior art since applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. Indeed, it has been held that optimization of range limitations are prima facie obvious absent such a disclosure. See MPEP 2144.05(II). Therefore,

it would have been obvious to one having ordinary skill in the art to select the output capacitance to be 1 uF dependent upon particular environment of use to ensure optimum performance.

As to claim 14, the modified Kandaka's figure 2 shows a method of stabilization of a circuit having a capacitive load (40) on the order of approximately 1uF and having two current loop sub circuits comprising the steps of: providing a main current loop (loop comprising 12, 50, R1, R2, 40) for supplying current to the load, the main current loop having a first compensation capacitance (capacitor C11 in Chen's figure 1) for maintaining stability within a pre-selected operational range; providing sensing loop (loop comprising 22, 16, 14) for monitoring the current to the load, the sensing loop having a second compensation capacitance (14) for maintaining stability within a pre-selected operational range; and coupling the output of the main current loop and the output of the sensing loop such that the first compensation capacitance is isolated from the second compensation capacitance.

As to claim 15, the modified Kandaka's figure 2 shows that the output of the main current loop is coupled to the gate of a transistor (18) and the output of the sensing loop is coupled to the source of the transistor.

As to claim 16, the modified Kandaka's figure 2 shows that the output of the main loop further comprises an error amplifier (12) and wherein the output of the main loop comprises a low impedance node of the error amplifier.

As to claim 17, the modified Kandaka's figure 2 shows that the main loop further comprises an error amplifier and wherein the output of the main loop comprises a high impedance node of the error amplifier.

As to claim 18, Kandaka's figure 2 is used in a low dropout regulator (LDO).

Claims 1-5 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Primary Examiner

June 2, 2005